WEDNESDAY, 14th May 2025		
8:30 – 9:00	Welcome coffee	
9:00 – 9:10	OPENING SESSION	
9:10 – 9:50	INVITED TALK 1 Pursuing the FD-SOI roadmap down to 10-7 nm nodes for high Energy Efficient, Low Power and RF/mmWave applications – Claire Fenouillet-Beranger (CEA-LETI) Chair: TBA	
9:50 – 10:00	Conclusions of ICOS Workshop – Giorgios Fagas (Tyndall)	
10:00 – 10:20	Coffee Break	
10:20 – 12:00	SESSION 1 – "Advanced SOI materials and devices, part I" Chair: TBA	
10:20 – 10:40	300 mm sSOI engineering with UltraThin BOX – David Barge (CEA-LETI)	
10:40 – 11:00	Effect of PN Passivation on MOSFETs Performance in 28 nm FD-SOI – Martin Vanbrabant (UCLouvain)	
11:00 – 11:20	3D simulation of charge defect impact on an industrial 28 nm FD-SOI quantum dot – Benjamin Bureau (STM)	
11:20 – 11:40	Integration of W vias for individual coupling control in 28nm FD-SOI qubit arrays – Giselle Elbaz (Quobly)	
11:40 – 12:00	Toward Full Relaxation of sSOI Substrates for PFET Device Fabrication - Nguyet Phuong TRAN (CEA-LETI)	
12:00 – 13:20	Lunch	
13:20 – 14:40	SESSION 2 – "Innovative devices: simulation and compact modeling" Chair: TBA	
13:20 – 13:40	Simulation of hole spin qubits in SOI quantum dots: comparison between different geometries – Lorenzo Raschi (University of Bologna)	
13:40 – 14:00	Superimposed Two-contact Gate Stacks for an Improved Electrostatic Control of Si Spin Qubits – Biel Martinez i Diaz (CEA-LETI)	
14:00 – 14:20	Model of Threshold Voltage and Drain Current in Core-Shell Junctionless Transistor on FD-SOI – Cunhua Dou (Nanjing University of Posts and Telecommunications)	
14:20 – 14:40	Compact I-V Modeling of Short Channel MoS2 FETs: A Physics-Based Approach – Ahmed Mounir (Rovira i Virgili University)	
14:45 – 15:45	**POSTER short presentations** Chair: TBA	
15:45 – 18:00	Coffee break & **Poster session**	**EID Panel** (15:45 – 16:15) Chair: Carmen Moldovan (CINTECH)
19:30 – 23:00	Welcome cocktail @"W Orbicie Słońca"	

THURSDAY, 15th May 2025	
9:00 – 10:40	SESSION 3 – "Advanced SOI materials and devices, part II" Chair: TBA
9:00 – 9:20	Low-loss RF substrate compatible with FD-SOI integration using Si+ implantation – Martin Perrosé (CEA-LETI)
9:20 – 9:40	On the role of Power dissipation in the Post-BD Behavior of FDSOI NanoWire FETs – Rishab Goyal (Autonoma University of Barcelona)
9:40 – 10:00	Stress Enhancement and Relaxation Minimization in Locally Strained SOI with the STRASS Technique – Louis-David MOHGOUK ZOUKNAK (CEA-LETI)
10:00 – 10:20	A Schottky Barrier Field-Effect Transistor Platform with Variable Ge Content on SOI – Andreas Fuchsberger (TU Wien)
10:20 – 10:40	Electrically controlled switching of the magnetic orientation in Mn3Sn and CoFeB – B Pruckner (Christian Doppler Laboratory for Nonvolatile Magnetoresistive Memory and Logic)
10:40 – 11:00	Coffee break
11:00 – 12:40	SESSION 4 – "New channel materials for CMOS electronics" Chair: TBA
11:00 – 11:40	INVITED TALK 2 2D semiconductors for future computing – Xinran Wang (Nanjing University)
11:40 – 12:00	Plasma-Enhanced ALD Growth of 2D Devices on SiO2/Si Wafer Substrates – Carlos Marquez (University of Granada)
12:00 – 12:20	Design guidelines for Gr-MoS2 based DS-FETs – Tommaso Ugolini (University of Bologna)
12:20 – 12:40	ITO Interconnects for Transparent Electronics – Doga Selin Memikoglu (KTH)
12:40 – 14:00	Lunch
14:00 – 15:40	SESSION 5 – "Memory devices and structures" Chair: TBA
14:00 – 14:40	INVITED TALK 3 Scaling and Innovations of DRAM Technology for the AI-Driven Future – Minsoo Yoo (SK Hynix Inc.)
14:40 – 15:00	Nor-type Gated Diode Synapse Array with Selective Program/Erase Operation Capabilities – Kyu-Ho Lee (Seoul National University)
15:00 – 15:20	Analog Resistive Switching Phenomena in Titanium Oxide Thin-Film Memristive Devices – Karimul Islam (WUT)
15:20 – 15:40	A Closed-Form Model for Programming of Oxide-Based Resistive Random Access Memory Cells Derived From the Stanford Model – Nadine Dersch (THM University of Applied Sciences)
15:40 – 16:00	Coffee break

16:00 – 17:00	SESSION 6 – “Biosensors” Chair: TBA
16:00 – 16:20	Silicon Nanowire Field-Effect Transistor Biosensors with Bowtie Antenna – Svetlana Vitusevich (Forschungszentrum Juelich)
16:20 – 16:40	Influence of Gate Capacitance Ratio on ISFET Memory – Henrique Lanfredi Carvalho (University of Sao Paulo)
16:40 – 17:00	Graphene-enabled glucose sensing: From field-effect transistors to next-generation wearables – Vicente Silva Lopes (INL)
19:00 – 23:00	Excursion + Gala dinner @Bazyliszek, “The Old Town”

FRIDAY, 16th May 2025	
9:00 – 10:40	SESSION 7 – "Device simulation, characterization, and compact modeling, part I", Chair: TBA
9:00 – 9:20	Geometrical Variability Impact on the Gate Tunneling Leakage Mechanisms in FinFETs – Cristina Medina-Bailon (University of Granada)
9:20 – 9:40	Coverage Ratio of Bottom Channel on Intrinsic Device Characteristics of GAA Si NS CFETs – Min-Hui Chuang (National Yang Ming Chiao Tung University)
9:40 – 10:00	Band Structure-based Estimation of Radiation Tolerance and Reliability of UTB MOS Devices – Nalin Vilochan Mishra (Indian Institute of Science Education and Research)
10:00 – 10:20	MULHACEN, enhanced multi-subband Monte Carlo simulator for non-planar FETs – Cristina Medina-Bailon (University of Granada)
10:20 – 10:40	DC Parameter Analysis of Asymmetric VNW JL GAA pMOSFETs on SOI from 300K to 400K – Abderrahim TAHIAT (ENSICAEN)
10:40 – 11:00	Coffee break
11:00 – 12:40	SESSION 8 – "Device simulation, characterization, and compact modeling, part II", Chair: TBA
11:00 – 11:40	INVITED TALK 4 Wide Bandgap Energy Efficient Devices and Their Applications – Mikael Ostling (KTH)
11:40 – 12:00	Statistical Enhancement in Two-particle Device Monte Carlo – Josef Gull (Institute for Microelectronics)
12:00 – 12:20	Monte Carlo analysis of hot electron injection in the passivation layer above GaN HEMTs – Pierpaolo Palestri (University of Modena)
12:20 – 12:40	A Methodology for PDK Re-Centering Using TCAD and Experimental Data for Cryogenic Temperatures – Tapas Dutta (Semiwise Ltd.)
12:40 – 13:20	Lunch
13:20 – 14:40	SESSION 9 – "Alternative transistors architectures and variability" Chair: TBA
13:20 – 13:40	Experimental Investigation of 7-Level Stacked Nanosheet nMOSFETs for High-Temperature Applications – Michelly de Souza (Centro Universitário FEI)
13:40 – 14:00	Application of Forksheet Transistor in Operational Transconductance Amplifier – Joao Martino (University of Sao Paulo)
14:00 – 14:20	Assessing the Impact of Process and Design Variations on Reliability of Complementary FET – Ankit Dixit (University of Glasgow)
14:20 – 14:40	Fracture dynamics in Smart Cut technology: Wafer deformation measurement – Lucas Colonel (CEA-LETI)
14:40 – 15:00	Conference closing and coffee break